Notice of References Cited	Application/Control No. 10/676,929	Applicant(s)/Patent Under Reexamination SINGH, AMIT	
	Examiner Tuyen To	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,813,754	11-2004	Wu et al.	716/10
	B	US-5,475,830	12-1995	Chen et al.	716/16
	C	US-6,099,580	08-2000	Boyle et al.	716/7
	D	US-2004/0250226	12-2004	Lin et al.	716/007
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Russo, R.L.; Wolff, P.K., Sr.,"A computer-based-design approach to partitioning and mapping of computer logic graphs" Proceedings of the IEEE ,Volume 60, Issue 1, Jan. 1972 Page(s):28 - 34 □□
	V	G. Parthasarathy, M. Marek-Sadowska, Arindam Mukherjee, Amit Singh, "Interconnect Complexity-Aware FPGA Placement Using Rent's Rule ", March 2001 Proceedings of the 2001 international workshop on System-level interconnect prediction
	W	Amit Singh, Ganapathy Parthasarathy, Malgorzata Marek-Sadowska, " Interconnect Resource-Aware Placement for Hierarchical FPGAs", November 2001 Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design.
	X	Alexander (Sandy) Marquardt, Vaughn Betz, Jonathan Rose, "Using cluster-based logic blocks and timing-driven packing to improve FPGA speed and density" February 1999, Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.